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**PATENT APPLICATION**
**ATTORNEY DOCKET NO. A7544**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**



In re application of

Jörg HENKEL, et al.

Appln. No. Group Art Unit:

Filed: January 24, 2000 Examiner:

For: METHOD FOR CORE-BASED SYSTEM-LEVEL POWER MODELING USING OBJECT-ORIENTED TECHNIQUES

**INFORMATION DISCLOSURE STATEMENT**
**UNDER 37 C.F.R. §§ 1.97 and 1.98**

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached Form PTO-1449 and listed herein and which the Examiner may deem relevant to patentability of the claims of the above-identified application.

1. A. Raghunathan, S. Dey and N. K. Jha, *Glitch Analysis And Reduction In Register-Transfer-Level Power Optimization*, IEEE Proc. of Design Automation Conference (DAC96), pp. 331-336 (1996).

2. A. Chandrakasan, M. Potkonjak, J. Rabaey and R. Brodersen, *Hyper-LP: A System for Power Minimization using Architectural Transformations,* IEEE Proc. of Int'l Conf. on Computer-Aided Design (IC-CAD92), pp. 300-303 (1992).

3. G. Lakshminarayana, A. Raghunathan, K. S. Khouri and N. K. Jha, *Common Case Computation: A High-Level Power-Optimizing Technique,* IEEE Proc. of Design Automation Conference (DAC99), June 1999.

4. S. Kumar, J. Aylor, B. Johnson and W. Wuif, *Object-Oriented Techniques in Hardware Design,* IEEE Computer, Vol. 27, pp. 64-70 (June 1994).

5. F. Mallet, F. Hoed, and J. F. Duboc, *Hardware Architecture Modeling Using an Object-Oriented Method,* Proceedings of the 24th EUROMICRO Conference, August 1998.

6. C. Passerone, R. Passerone, C. Sansoe, J. Martin, A. Sangiovanni-Vincentelli and R. McGeer, *Modeling Reactive Systems in Java,* Proceedings of the Sixth International Workshop on Hardware/Software Codesign, March 1998.

7. J. S. Young, J. MacDonald, M. Shilman, A. Tabbara, P. Hilfinger and A. R. Newton, *Design and Specification of Embedded Systems in Java Using Successive Format Refinement,* Proceedings of the Design and Automation Conference, June 1998.

8. F. Vahid and T. Givargis, *Incorporating Cores into System-Level Specification,* International Symposium on System Synthesis, December 1998.

9. T. Givargis and F. Vahid, *Interface Exploration for Reduced Power in Core-Based Systems,* International Symposium on System Synthesis, December 1998.

10. T. Givargis, J. Henkel and F. Vahid, *Interface and Cache Power Exploration for Core-Based Embedded System Design,* Submitted to International Conference on Computer Aided Design, November 1999.

11. W. Fornaciari, D. Sciuto and C. Silvano, *Power Estimation for Architectural Explorations of HW/SW Communication on System-Level Buses*, To be published at HW/SW Codesign Workshop, Rome, May 1999.

12. Jue-Hsien Chem, Jean Huang, Lawrence Arledge, Ping-Chung Li and Ping Yang, *Multilevel Metal Capacitance Models for CAD Design Synthesis Systems,* IEEE Electron Device Letters, Vol. 13, No. 1, pp.32-34 (January 1992).

13. B. Payne, *Rapid Silicon Prototyping: Paradigm for Custom System-on-a-Chip Design,* http://www.vlsi.com/velocity, 1998.

14. A. Evans, A. Silburt, G. Vrckovnik, T. Brown, M. Dufresne, G. Hall, T. Ho and Y. Liu, *Functional Verification of Large ASICs,* Design Automation Conference, 1998.

15. R. Gupta and Y. Zorian, *Introducing Core-Based System Design,* IEEE Design and Test, Vol. 14, No. 4, pp. 15-25 (Oct-Dec 1997).

16. U.S. Patent No. 5,481,469 January 2, 1996 to Brasen, et al.

17. U.S. Patent No. 5,870,308 February 9, 1999 to Dangelo, et al.

18. U.S. Patent No. 5,572,436 November 5, 1996 to Dangelo, et al.

19. U.S. Patent No. 5,801,958 September 1, 1998 to Dangelo, et al.

20. U.S. Patent No. 5,696,694 December 9, 1997 to Khouja, et al.

21. U.S. Patent No. 5,682,320 October 28, 1997 to Khouja, et al.

22. U.S. Patent No. 5,838,579 November 17, 1998 to Olson, et al.

23. U.S. Patent No. 5,838,947 November 17, 1998 to Sarin

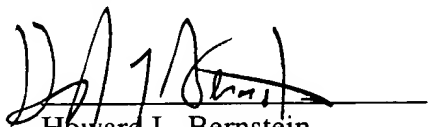
24. U.S. Patent No. 5,903,476 May 11, 1999 to Mauskar, et al.

One copy of each of the listed documents is submitted herewith.

The present Information Disclosure Statement is being filed concurrently with the filing of the present application, and therefore no Statement under 37 C.F.R. § 1.97(e) or fee under 37 C.F.R. § 1.17(p) is required.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicants do not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

Respectfully submitted,



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